CLAIMS

What is claimed is:

1. An integrated circuit comprising:

a semiconductor substrate;

an epitaxial layer coupled to the substrate, the oxide layer having been coupled to the substrate via a transfer process comprising:

doping the epitaxial layer with a first quantity of a first ionic material and a second quantity of a second ionic material;

annealing the epitaxial layer and semiconductor substrate at a first annealing temperature.

2. The integrated circuit of claim 1 wherein the sum of the first quantity of the first ionic material and the second quantity of the second ionic material is no greater than approximately $2x10^{16}$ cm^{-2}.

3. The integrated circuit of claim 1 wherein the first annealing temperature is between approximately 439 degrees C and approximately 451 degrees C.

4. The integrated circuit of claim 1 wherein the first annealing temperature is between approximately 419 degrees C and approximately 430 degrees C.

5. The integrated circuit of claim 4 wherein the process further comprises

mechanically separating a donor wafer, comprising the epitaxial layer, from a handle wafer, comprising the semiconductor substrate.

6. The integrated circuit of claim 2 wherein the second ionic material comprises hydrogen ions to react with the epitaxial layer at an energy level of approximately 40 KeV.

7. The integrated circuit of claim 6 wherein the first ionic material comprises helium ions to react with the epitaxial layer at an energy level of approximately 50 KeV.

8. The integrated circuit of claim 7 wherein the first quantity of helium ions is approximately 1×10^{16} cm^{-2} and the second quantity of hydrogen ions is approximately 1×10^{16} cm^{-2}.

9. A method comprising:

implanting a first wafer, including a substantially first layer, with a first quantity of helium ions and a second quantity of hydrogen ions;

introducing a surface of a second wafer, including a silicon substrate, to a surface of the first layer;

annealing the first layer and the silicon substrate at a first temperature for a first amount of time.

10. The method of claim 9 further including separating a portion of the first layer from the first wafer that is not bonded with the silicon substrate after the first amount of time.

11. The method of claim 10 wherein the sum of the first quantity of helium ions and the second quantity of hydrogen ions is no greater than approximately $2x10^{16}$ cm^{-2}.

12. The method of claim 11 wherein the first quantity of helium ions is no greater than approximately $1x10^{16}$ cm^{-2}.

13. The method of claim 11 wherein the second quantity of hydrogen ions is no greater than approximately $1x10^{16}$ cm^{-2}.

14. The method of claim 9 further comprising forming voids in the first layer as a result of the second quantity of hydrogen ions interacting with the substrate.

15. The method of claim 14 wherein the second quantity of hydrogen ions have an energy range of approximately 40 KeV.

16. The method of claim 15 wherein the first quantity of helium ions help the voids to expand at an energy level of approximately 50 KeV.

17. The method of claim 9 wherein the first temperature is approximately 440C and the first amount of time is approximately 10 minutes.

18. A process comprising:

forming an epitaxial layer on a donor wafer;

forming a film oxide on a handle wafer;

transferring a portion of the epitaxial layer to the handle wafer, the transferring including implanting the epitaxial layer with a first quantity of positively charged helium ions and a second quantity of positively charged hydrogen ions.

19. The process of claim 18 wherein the transferring further comprising performing an annealing process on the donor wafer and handle wafer while they are in direct contact with each other.

20. The process of claim 19 wherein the annealing temperature is no greater than approximately 430 degrees C.

21. The process of claim 18 wherein the sum of the first quantity helium ions and the second quantity of hydrogen ions is approximately $2x10^{16}$ cm^{-2}.

22. The process of claim 20 wherein the transferring further comprises using a

mechanical cleave process to separate a portion of the epitaxial layer from the handle wafer.

23. The process of claim 21 wherein the first quantity of helium ions is approximately $1x10^{16}$ cm^{-2}.

24. The process of claim 23 wherein the second quantity of hydrogen ions is approximately $1x10^{16}$ cm^{-2}.

25. The process of claim 18 wherein the film oxide comprises SiO_2.

26. The process of claim 25 wherein the epitaxial layer is chosen from a group consisting of silicon, Ge, GaAS, InP, GaN, GaSb, and InSb.

27. An apparatus comprising:

first means for creating voids in an oxide layer, the first means comprising a first quantity of a first type of ions;

second means for expanding the voids comprising a second quantity of a second type of ions;

third means for annealing the voids.

28. The apparatus of claim 27 wherein the first type of ions is chosen from

ions of a group of elements consisting of argon, neon, xenon, nitrogen, hydrogen, and helium.

29. The apparatus of claim 27 wherein the second type of ions is chosen from ions of a group of elements consisting of argon, neon, xenon, nitrogen, hydrogen, and helium.

30. The apparatus of claim 27 wherein the first quantity of the first type of ions comprises no greater than approximately 1×10^{16} cm^{-2} of hydrogen ions and the second quantity of the second type of ions comprises no greater than 1×10^{16} cm^{-2} of helium ions.

31. The apparatus of claim 27 wherein the first means further comprises an energy range of approximately 40 KeV and the second means comprises an energy range of approximately 50 KeV.

32. The apparatus of claim 27 wherein the third means comprises an ambient temperature of approximately 440 degrees C.

33. The apparatus of claim 27 further comprising a fourth means for separating a donor wafer, comprising the oxide layer, from a handle wafer, comprising a semiconductor substrate.

34. The apparatus of claim 31 wherein the fourth means comprises a thermal cleave process if the third means comprises an ambient temperature of at least approximately 440 degrees C.

35. The apparatus of claim 31 wherein the fourth means comprises a mechanical cleave process if the third means comprises an ambient temperature of no greater than approximately 430 degrees C.